

10/567991

Attorney's Docket No.: 19415-007US1 / PCT-04R-166/US

JAP20 Res'd PCT/PTO 09 FEB 2006

**APPLICATION
FOR
UNITED STATES LETTERS PATENT**

TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

APPLICANT: HIDETOSHI NISHIKAWA

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. ET931348400US

February 9, 2006

Date of Deposit

SPECIFICATION**SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE****Technical Field**

[0001] The present invention relates to a semiconductor integrated circuit device built as a shift register that converts inputted serial data into parallel data, more particularly, relates to a semiconductor integrated circuit device provided with a plurality of shift registers.

Background Art

[0002] Conventionally, in printer head drivers or the like, shift registers are provided that receive data on a bit-by-bit basis as serial data and store it therein. In this shift register, the inputted serial data is divided on a bit-by-bit basis, then converted into parallel data, and then fed to a latch circuit. Each bit of data, having been stored in the latch circuit, is then outputted from the latch circuit to a drive circuit with predetermined timing determined on a bit-by-bit-basis, permitting electric current to be fed to a heating resistance or a light-emitting element.

[0003] As a printing apparatus provided with such a conventional printer head driver, there has been proposed a printing apparatus in which a plurality of heating elements are divided into a plurality of blocks, and a plurality of shift registers of the same number of bits as the number of heating elements of each block are provided (see Patent Publication 1). In this printing apparatus, data of each block is stored in each

shift register, and the individual shift registers are driven with different timing. This makes it possible to separate a shift register performing data output and a shift register performing data input, making it possible to speed up printing operation.

[0004] As described above, when a shift register is provided on a block-by-block basis, a plurality of shift registers are built in a semiconductor integrated circuit device. Specifically, as shown in Fig. 8, a 64-bit shift register SRX composed of flip-flops FF1 to FF64 and a 64-bit shift register SRY composed of flip-flops FF65 to FF128 are built in a single semiconductor integrated circuit device 100. Now, the semiconductor integrated circuit device 100 has an input terminal SI1 that receives serial data to the shift register SRX, a clock input terminal CLK that receives a clock, an output terminal SO1 that outputs serial data from the shift register SRX, and an input terminal SI2 that receives serial data to the shift register SRY. Moreover, the flip-flop FF1 of the shift register SRX and the flip-flop FF65 of the shift register SRY each have, on the input side thereof, an input driver Din, and the flip-flop FF64 of the shift register SRX has, on the output side thereof, an output driver Dout.

Patent Publication 1: Japanese Patent Application Laid-Open No. H5-229159

Disclosure of the Invention

Problems to be Solved by the Invention

[0005] However, in the semiconductor integrated circuit device 100 built with the shift registers SRX and SRY as shown in Fig. 8, when the shift register SRX and the shift register SRY are used as a 128-bit shift register by inputting serial data from the former to the latter, it is necessary to connect the output terminal SO1 and the input

terminal SI2 together via an external conductor laid on a substrate outside the semiconductor integrated circuit device 100. This leads to a delay in transferring data from the output buffer Dout of the shift register SRX to the input buffer Din of the shift register SRY via an external parasitic load capacitance such as an external conductor laid on a substrate.

[0006] In this case, a relationship between a clock to be inputted from the clock input terminal CLK, an input si64 and an output so64 of the flip-flop FF64, and an input si65 and an output so65 of the flip-flop FF65 is shown in Fig. 9 or 10. Specifically, in a case where the clock frequency is low as shown in Fig. 9, when a set-up time t elapses from when the clock varying as shown in Fig. 9(a) rises to high level, the flip-flop FF64 changes the output so64, as shown in Fig. 9(c), to a value corresponding to a value taken by the input si64 when the clock rises to high level as shown in Fig. 9(b).

[0007] Then, as shown in Fig. 9(d), the output so64 from the flip-flop FF64 is delayed by time td , and is then inputted as the input si65 to the flip-flop FF65, which changes the output so65 as shown in Fig. 9(e), as with the flip-flop FF64, when the set-up time t elapses from when the clock rises to high level, to a value corresponding to a value taken by the input si65 when the clock rises to high level as shown in Fig. 9(d).

[0008] In the example shown in Fig. 9, the clock frequency is low as shown in Fig. 9(a), and its cycle T is longer than the sum of set-up time t and delay time td ($= t + td$). This makes it possible to make the output so65 of the flip-flop FF65 correspond to the output so64 of the flip-flop 64. Therefore, it is possible to operate the shift registers SRX and SRY without loss of data.

[0009] Now, suppose that, as shown in Fig. 10(a), the clock frequency is made higher,

and its cycle T is made shorter than the sum of set-up time t and delay time td ($= t + td$). Then, the input si64 and the output so64 behave as shown in Figs. 10(b) and 10(c), respectively, whereby the flip-flop FF64 can operate corresponding to the clock. However, the input si65 to the flip-flop FF65 behaves as shown in Fig. 10(d), whereby the input si65 changes after rising of the clock. As a result, as shown in Fig. 10(e), the output so65 of the flip-flop FF65 does not correspond to the output so64 from the flip-flop FF64, leading to data loss in the flip-flop FF65.

Means for Solving the Problem

[0010] In view of the conventionally experienced problems described above, an object of the present invention is to provide a semiconductor integrated circuit device that is built with a plurality of shift registers, and that permits the shift registers, when they are made to operate with the output of one shift register connected to the input of another, to operate without malfunctioning even at a high frequency.

[0011] To achieve the above object, according to one aspect of the present invention, a semiconductor integrated circuit device is provided with: first to n-th shift registers; first to n-th input terminals that receive data fed to the first to n-th shift registers; a first switch that electrically connects and disconnects the output of a k-th shift register (where k is an integer such that $1 \leq k \leq n-1$) and the input of a k+1-th shift register; a second switch that electrically connects and disconnects the input of the k+1-th shift register and a k+1-th input terminal that receives data to the k+1-th shift register; and a selection signal input terminal that receives a selection signal for switching ON/OFF of the first switch and the second switch. When the k-th shift register and the k+1-th

shift register are used in a combined manner, the first switch is turned ON and the second switch is turned OFF by the selection signal. On the other hand, when the k-th shift register and the k+1-th shift register are used separately, the first switch is turned OFF and the second switch is turned ON by the selection signal.

[0012] According to another aspect of the present invention, a semiconductor integrated circuit device is provided with: first to n-th shift registers; first to n-th input terminals that receive data fed to the first to n-th shift registers; and a switching control portion that performs, according to whether or not a k+1-th input terminal that receives data to a k+1-th shift register (where k is $1 \leq k \leq n-1$) is connected to the outside, switching control of whether the output of the k-th shift register and the input of the k+1-th shift register are connected together, or the k+1-th input terminal and the input of the k+1-th shift register are connected together. When the switching control portion recognizes that the k+1-th input terminal is in an open state in which the k-th input terminal is not connected to the outside, the output of the k-th shift register and the input of the k+1-th shift register are connected together, and the k+1-th input terminal and the input of the k+1-th shift register are disconnected from one another. When the switching control portion recognizes that the k+1-th input terminal is connected to the outside and data is inputted thereto, the output of the k-th shift register and the input of the k+1-th shift register are disconnected from one another, and the k+1-th input terminal and the input of the k+1-th shift register are connected together.

Effect of the Invention

[0013] According to the present invention, a plurality of shift registers are provided, among which the output of a shift register can be internally connected to the input of the adjacent one, eliminating the need to connect them together via an external conductor laid on a substrate as in the conventional example. Therefore, unlike the conventional example, it is possible to prevent a delay between the shift registers caused by the influence of an external parasitic load capacitance or the like. This permits the shift registers, even when the adjacent ones are made to operate in a combined manner, to operate with high frequency clock. Moreover, according to the present invention, by feeding an input from the outside to the individual shift registers or making the number of signals coming from the outside smaller than the number of shift registers, it is possible to select whether or not to connect the input of one shift register with the output of another. This makes it possible to select whether the shift registers inside the semiconductor integrated circuit device are used separately or in a combined manner.

[0014] Moreover, according to the present invention, it is possible to replace an output terminal required in the conventional example to output an output from each shift register to the outside with a selection signal input terminal. Therefore, as compared with the conventional semiconductor integrated circuit device, it can be realized without increasing the number of terminals. Furthermore, by making it possible to perform switching according to whether or not an input terminal is connected to the outside, it is possible to omit the selection signal input terminal that receives a selection signal, thereby reducing the number of terminals.

Brief Description of Drawings

[0015] [Fig. 1] A block circuit diagram showing the internal configuration of the semiconductor integrated circuit device provided with the shift registers of a first embodiment.

[Fig. 2] A circuit diagram showing the configuration of the transistor switch.

[Fig. 3] A block circuit diagram showing another example of the internal configuration of the semiconductor integrated circuit device provided with the shift registers of the first embodiment.

[Fig. 4] A block circuit diagram showing the internal configuration of the semiconductor integrated circuit device provided with the shift registers of a second embodiment.

[Fig. 5] A block circuit diagram showing another example of the internal configuration of the semiconductor integrated circuit device provided with the shift registers of the second embodiment.

[Fig. 6] A diagram showing the configuration of the resistance that is composed of the MOS transistors and that is included in the semiconductor integrated circuit device of Fig. 5.

[Fig. 7] A block circuit diagram showing the internal configuration of another example of the semiconductor integrated circuit device provided with the shift registers of the second embodiment.

[Fig. 8] A block circuit diagram showing the internal configuration of the semiconductor integrated circuit device provided with conventional shift registers.

[Fig. 9] A timing chart partially showing the operation performed inside the semiconductor integrated circuit of Fig. 7.

[Fig. 10] A timing chart partially showing the operation performed inside the semiconductor integrated circuit of Fig. 7.

List of Reference Symbols

[0016]	1, 1a, 1b	semiconductor integrated circuit device
	2, 20	switching control portion

Best Mode for Carrying Out the Invention

[First embodiment]

[0017] A first embodiment of the present invention will be described with reference to the drawings. Fig. 1 is a block circuit diagram showing the internal configuration of the semiconductor integrated circuit device of this embodiment.

[0018] A semiconductor integrated circuit device 1 of Fig. 1 includes: a 64-bit shift register SR1 composed of flip-flops FF1 to FF64 and an input driver Din1; a 64-bit shift register SR2 composed of flip-flops FF65 to FF128; an input terminal SI1 that receives serial data to the shift register SR1; a clock input terminal CLK that receives a clock; an input terminal SI2 that receives serial data to the shift register SR2; an input driver Din2 connected to the input terminal SI2; a transistor switch SWA that electrically connects and disconnects the output of the flip-flop FF64 and the input of the flip-flop FF65; a transistor switch SWB that electrically connects and disconnects the output of the input driver Din2 and the input of the flip-flop FF65; a selection

signal input terminal SEL that receives a selection signal for controlling ON/OFF of the switches SWA and SWB; and an inverter Inv connected to the selection signal input terminal SEL.

[0019] As shown in Fig. 2, the transistor switches SWA and SWB are each composed of a P-channel MOS transistor Tp and an N-channel MOS transistor Tn connected in parallel. In the transistor switch SWA, a selection signal inverted by the inverter Inv is inputted to the gate of the MOS transistor Tp, and a selection signal inputted via the selection signal input terminal SEL is inputted to the gate of the MOS transistor Tn. In the transistor switch SWB, a selection signal inverted by the inverter Inv is inputted to the gate of the MOS transistor Tn, and a selection signal inputted via the selection signal input terminal SEL is inputted to the gate of the MOS transistor Tp.

[0020] When such a connection is established and a 128-bit shift register is built with the shift registers SR1 and SR2, high level is inputted from the selection signal input terminal SEL as a selection signal, the switch SWA turns ON, and the switch SWB turns OFF. Accordingly, the data outputted from the flip-flop FF64 of the shift register SR1 is inputted to the input of the flip-flop FF65 via the switch SWA.

[0021] As a result, inside the semiconductor integrated circuit device 1, the output of the flip-flop FF64 and the input of the flip-flop FF65 are connected together. Therefore, unlike the conventional configuration as shown in Fig. 8, it is possible to omit an output driver Dout and an input driver Din lying between the output of the flip-flop FF64 and the input of the flip-flop FF65, and there is no need to connect them together via an external conductor laid on a substrate outside the semiconductor integrated circuit device. This makes it possible to prevent a delay between the

output of the flip-flop FF64 and the input of the flip-flop FF65.

[0022] On the other hand, when two 64-bit shift registers are built with the shift registers SR1 and SR2 in such a way that data is inputted to the shift registers SR1 and SR2 from the input terminals SI1 and SI2, respectively, low level is inputted from the selection signal input terminal SEL as a selection signal, the switch SWA turns OFF, and the switch SWB turns ON. As a result, data inputted from the input terminal SI2 is inputted to the input of the flip-flop FF65 via the input driver Din2 and the switch SWB.

[0023] With this configuration, when a plurality of shift registers built in the semiconductor integrated circuit device 1 are used in a combined manner as a single shift register, switching a selection signal makes it possible to prevent a data delay between the input of a shift register and the output of the adjacent one. Therefore, even when a clock frequency is made higher, it is possible to prevent data loss between the input of a shift register and the output of the adjacent one. Moreover, it is possible to replace an terminal used in the conventional configuration as shown in Fig. 8 as an output terminal SO1 with a selection signal input terminal SEL, making it possible to achieve this configuration by using as many terminals as those of the conventional one.

[0024] This embodiment deals with a case where two 64-bit shift registers are built in the semiconductor integrated circuit device 1. It should be understood, however, that a shift register of a different number of bits may be used instead of a 64-bit shift register. Moreover, it should be understood that, instead of a transistor switch, a switch having a different configuration may be used as the transistor switches SWA

and SWB.

[0025] Furthermore, as shown in Fig. 3, it may be built with n shift registers SR1 to SRn, and there may be provided switches $n-1$ SWA1 to SWAn-1 and $n-1$ switches SWB1 to SWBn-1 between the adjacent shift registers. In this case, there are provided $n-1$ selection signal input terminals SEL1 to SELn-1 and $n-1$ inverters Inv1 to Invn-1, and selection signals and inverted selection signals fed therefrom are respectively inputted to the switches SWA1 to SWAn-1 and the switches SWB1 to SWBn-1.

[0026] Moreover, input terminals SI2 to SIn and input drives Din2 to DInn are used when data is inputted to the shift registers SR2 to SRn from the outside. Therefore, by switching ON/OFF of the switches SWA1 to SWAn-1 and the switches SWB1 to SWBn-1 according to a selection signal, it is possible to build a shift register of a desired number of bits by decoupling or coupling the shift registers SR1 to SRn.

[0027] It should be understood that the number of selection signal input terminals may be made smaller than $n-1$, and there may be provided a switching control portion that controls switching of the switches SWA1 to SWAn-1 and SWB1 to SWBn-1 according to the number of pulses of a selection signal inputted to the selection signal input terminal.

[Second Embodiment]

A second embodiment of the present invention will be described with reference to the drawings. Fig. 4 is a block circuit diagram showing the internal configuration of the semiconductor integrated circuit device of this embodiment. It

is to be noted that, in the semiconductor integrated circuit device shown in Fig. 4, such components used for the same purpose as their counterparts in the semiconductor integrated circuit device shown in Fig. 1 are identified with the same reference numerals, and their detailed descriptions will be omitted.

[0028] A semiconductor integrated circuit device 1a shown in Fig. 4 includes shift registers SR1 and SR2, input terminals SI1 and SI2, a clock input terminal CLK, an input driver Din2, a transistor switch SWA, a transistor switch SWB, a switching control portion 2 that generates, according to a state of the input terminal SI2, a selection signal for controlling ON/OFF of the switches SWA and SWB, and sends a signal inputted to the input terminal SI2 to the input driver Din2, and an inverter Invx that inverts a selection signal from the switching control portion 2. A selection signal from the switching control portion 2 is inputted to the gate of the MOS transistor Tp of the switch SWA and the gate of the MOS transistor Tn of the switch SWB, and a selection signal inverted by the inverter Invx is inputted to the gate of the MOS transistor Tn of the switch SWA and the gate of the MOS transistor Tp of the switch SWB.

[0029] In the semiconductor integrated circuit device 1a configured as described above, the switching control portion 2 operates according to the following three states:

- (1) a state in which the input terminal SI2 is not connected to the outside, and no data is inputted (a high-impedance state);
- (2) a state in which high level is inputted to the input terminal SI2 as data from the outside (a high-input state); and
- (3) a state in which low level is inputted to the input terminal SI2 as data from

the outside (a low-input state).

(1) In a high-impedance state

In this state, low level is outputted from the switching control portion 2 as a selection signal, whereby the switch SWA turns ON, and the switch SWB turns OFF. Therefore, data outputted from the flip-flop FF64 of the shift register SR1 is inputted to the input of the flip-flop FF65 of the shift register SR2 via the switch SWA. In this way, the shift registers SR1 and SR2 are coupled together, thereby forming a 128-bit shift register.

(2) In a high-input state

In this state, high level is outputted from the switching control portion 2 as a selection signal, whereby the switch SWA turns OFF, and the switch SWB turns ON. Furthermore, high level is inputted from the input terminal SI2 as data to the input of the flip-flop FF65 of the shift register SR2 via the input drive Din2 and the switch SWB.

(3) In a low-input state

In this state, low level is outputted from the switching control portion 2 as a selection signal, whereby the switch SWA turns OFF, and the switch SWB turns ON. Furthermore, low level is inputted from the input terminal SI2 as data to the input of the flip-flop FF65 of the shift register SR2 via the input drive Din2 and the switch SWB.

[0030] As described in (2) or (3), when data is inputted to the input terminal SI2 from the outside, the data from the outside is inputted to the input of the flip-flop FF65 of the shift register SR2 via the switching control portion 2, the input drive Din2, and the

switch SWB. In this way, the shift registers SR1 and SR2 are decoupled, thereby forming two separate 64-bit shift registers.

[0031] With this configuration, as compared with the semiconductor integrated circuit device 1 of the first embodiment, the semiconductor integrated circuit device 1a of this embodiment allows the selection signal input terminal SEL that receives a selection signal to be omitted. It is to be noted that, instead of a transistor switch, a switch having a different configuration may be used as the transistor switches SWA and SWB.

(Another example of the configuration of this embodiment)

Fig. 5 shows another example of the configuration of this embodiment. With this configuration, it is possible to omit a transistor switch SWB. A semiconductor integrated circuit device 1b shown in Fig. 5 includes: resistances Ra and Rb each having one end connected to an input terminal SI2; inverters I1 to I3 each connected, on an input side thereof, to a node at which the resistances Ra and Rb are connected together; an inverter I4 that receives an output of the inverter I3; an EXOR circuit EX1 that receives outputs of the inverters I2 and I4; an inverter I5 that receives an output of the EXOR circuit EX1; an N-channel MOS transistor T1a and a P-channel MOS transistor T2a that receive, at the gates thereof, an output from the inverter I5; an N-channel MOS transistor T1b and a P-channel MOS transistor T2b that receive, at the gates thereof, an output of the EXOR circuit EX1; and a P-channel MOS transistor T3a and an N-channel MOS transistor T3b that receive, at the gates thereof, an output from the inverter I1.

[0032] In this configuration, a supply voltage VDD is applied to the other end of the resistance Ra, and the other end of the resistance Rb is grounded. Moreover, a threshold value of an input to the inverter I2 at which an output therefrom is turned from high level to low level is set at 3/4 VDD, and a threshold value of an input of the inverter I3 at which an output therefrom is turned from high level to low level is set at 1/4 VDD. Specifically, when an input to the inverter I2 is in a range of 0 to 3/4 VDD, high level is outputted, whereas when an input thereto is in a range of 3/4 VDD to VDD, low level is outputted. Moreover, when an input to the inverter I3 is in a range of 0 to 1/4 VDD, high level is outputted, whereas when an input thereto is in a range of 1/4 VDD to VDD, low level is outputted. Threshold values of an input to the inverters I1, I4, and I5 may be either 1/4 VDD or 3/4 VDD.

[0033] Furthermore, the drain of the MOS transistor T1a and the source of the MOS transistor T1b are connected to the output of the flip-flop FF64 of the shift register SR1, and the source of the MOS transistor T1a and the drain of the MOS transistor T1b are connected to the input of the flip-flop FF65 of the shift register SR2. Moreover, a direct-current voltage VDD is applied to the source of the MOS transistor T3a, and the source of the MOS transistor T2a is connected to the drain of the MOS transistor T3a. The source of the MOS transistor T3b is grounded, and the source of the MOS transistor T2b is connected to the drain of the MOS transistor T3b. The drains of the MOS transistors T2a and T2b are connected to the input of the flip-flop FF65 of the shift register SR2. In this configuration, the MOS transistors T1a and T1b together build transistor switch.

(1) In a high-impedance state

In this configuration, when the input terminal SI2 is in a high-impedance state in which no data is inputted thereto from the outside, VDD/2 obtained by dividing the direct-current voltage by the resistances Ra and Rb is inputted to the inverters I1 to I3. As a result, high level is outputted from the inverter I2, and low level is outputted from the inverter I3. This makes the inverter I4 that receives the output of the inverter I3 output high level, and the EXOR circuit EX1 that receives the outputs of the inverters I2 and I4 output low level, making the inverter I5 that receives the output of the EXOR circuit EX1 output high level.

[0034] Then, the output from the EXOR circuit EX1 that outputs low level is inputted to the gates of the MOS transistors T1b and T2b, turning the MOS transistor T1b ON, and the MOS transistor T2b OFF. Moreover, the output from the inverter I5 that outputs high level is inputted to the gates of the MOS transistors T1a and T2a, turning the MOS transistor T1a ON, and the MOS transistor T2a OFF. Therefore, in this case, the data outputted from the flip-flop FF64 is inputted to the flip-flop FF65 via the transistor switch built with the MOS transistors T1a and T1b.

(2) In a high-input state

When high level is inputted to the input terminal SI2 as data from the outside, this high level (corresponding to the VDD) is inputted as data to the inverters I1 to I3. Therefore, low level is outputted from the inverters I1 to I3, and high level is outputted from the inverter I4 that receives the output of the inverter I3, making the EXOR circuit EX1 that receives the outputs of the inverters I2 and I4 output high level. Furthermore, the inverter I5 that receives the output of the EXOR circuit EX1 outputs low level.

[0035] Then, the output from the EXOR circuit EX1 that outputs high level is inputted to the gates of the MOS transistors T1b and T2b, turning the MOS transistor T1b OFF, and the MOS transistor T2b ON. Moreover, the output from the inverter I5 that outputs low level is inputted to the gates of the MOS transistors T1a and T2a, turning the MOS transistor T1a OFF, and the MOS transistor T2a ON.

[0036] Furthermore, the output from the inverter I1 that outputs low level is inputted to the gates of the MOS transistors T3a and T3b, turning the MOS transistor T3a ON, and the MOS transistor T3b OFF. Therefore, in this case, the supply voltage VDD (high level) is inputted to the flip-flop FF65 via the MOS transistors T2a and T3a.

(3) In a low-input state

When low level is inputted to the input terminal SI2 as data from the outside, this low level (corresponding to 0) is inputted as data to the inverters I1 to I3. Therefore, the inverters I1 to I3 output high level, and the inverter I4 that receives the output of the inverter I3 outputs low level, making the EXOR circuit EX1 that receives the outputs of the inverters I2 and I4 output high level. Furthermore, the inverter I5 that receives the output of the EXOR circuit EX1 outputs low level.

[0037] Then, the output from the EXOR circuit EX1 that outputs high level is inputted to the gates of the MOS transistors T1b and T2b, turning the MOS transistor T1b OFF, and the MOS transistor T2b ON. Moreover, the output from the inverter I5 that outputs low level is inputted to the gates of the MOS transistors T1a and T2a, turning the MOS transistor T1a OFF, and the MOS transistor T2a ON.

[0038] Furthermore, the output from the inverter I1 that outputs high level is inputted to the gates of the MOS transistors T3a and T3b, turning the MOS transistor T3a OFF,

and the MOS transistor T3b ON. Therefore, in this case, a ground voltage (low level) is inputted to the flip-flop FF65 via the MOS transistors T2b and T3b.

[0039] As described in (2) or (3), when data is inputted to the input terminal SI2 from the outside, the transistor switch built with the MOS transistors T1a and T1b is turned OFF, and the data from the outside is inputted to the input of the flip-flop FF65 of the shift register SR2 via the inverter I1 and the MOS transistors T2a, T2b, T3a, and T3b. In this way, the shift registers SR1 and SR2 are decoupled, thereby forming two separate 64-bit shift registers.

[0040] In this configuration, as shown in Fig. 6, the resistances Ra and Rb each may be composed of a P-channel MOS transistor Ta having a gate grounded and a source to which a supply voltage VDD is applied, and an N-channel MOS transistor Tb having a gate to which a supply voltage VDD is applied and a source grounded. The drains of these MOS transistors Ta and Tb are connected together, and a node at which they are connected together is connected to the inputs of the inverters I1 to I3.

[0041] With the configuration shown in Fig. 5, as compared with the semiconductor integrated circuit device 1 of the first embodiment, it is possible to omit a selection signal input terminal SEL that receives a selection signal, a transistor switch SWB, and an input drive Din2.

[0042] This embodiment deals with a case in which two 64-bit shift registers are built in the semiconductor integrated circuit device 1. It should be understood, however, that a shift register of a different number of bits may be used instead of a 64-bit shift register.

[0043] Furthermore, as shown in Fig. 7, it may be built with n shift registers SR1 to

SR_n, and there may be provided with $n-1$ switches SWA₁ to SWA_{n-1} and $n-1$ switches SWB₁ to SWB_{n-1} between the adjacent shift registers. Moreover, the input terminals SI₂ to SI_n and the input drives Din₂ to DIn_n are used when data is inputted to the shift registers SR₂ to SR_n from the outside.

[0044] In this case, there are provided a switching control portion 20 connected to the input terminals SI₂ to SI_n, and $n-1$ inverters Invx₁ to Invx_{n-1} to which $n-1$ selection signals from the switching control portion 20 are inputted, and the selection signals fed from the switching control portion 20 and the selection signals inverted by the inverters Invx₁ to Invx_{n-1} are inputted to the switches SWA₁ to SWA_{n-1} and the switches SWB₁ to SWB_{n-1}. Therefore, by switching ON/OFF of the switches SWA₁ to SWA_{n-1} and the switches SWB₁ to SWB_{n-1} according to a state of the input terminals SI₂₋₁ to SI_{2-n-1}, it is possible to build a shift register of a desired number of bits by decoupling or coupling the shift registers SR₁ to SR_n.

[0045] Furthermore, there may be provided $n-1$ logic circuits as shown in Fig. 5, each being composed of the inverters I₁ to I₅, the EXOR circuit EX₁, and the MOS transistors T_{1a} to T_{3a} and T_{1b} to T_{3b}, and lying between the input of a shift register and the output of the adjacent one of n shift registers SR₁~SR_n, and one input terminal for each logic circuit.